Electronics (II)

Term Project

106033110 李建鋒
106033125 邱郁茹
106030009 葉蓁

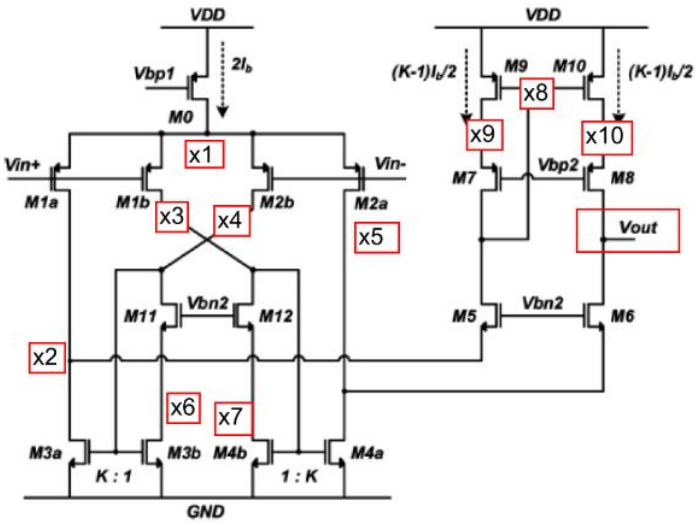


Fig.1

Node names

1. Design a two-stage operational amplifier

(a)Hand calculations

First, we have read some paper regarding the “recycling and folded cascode(RFC)”, and the recommend range of K is 2 to 4, so we pick 3 as a conservative choice.

After determining K, we first use the power spec (Pdiss <= 400 μW), and decide the value of bias current Ib. Since P = Vdd*(2Ib + 2* (333.-1)Ib/2), Vdd = 3, so Ib <= 33.33 μA，we set Ib = 30 μA to ensure the power would not be to high.

Then, through Vout range and ICMR, we set some boundary for Vov:

ICMR: $V_{ov3} + V_{tn} - |V_{tp}| = 0.5\ V$

$V_{DD} - V_{ov0} - V_{ov1a} - |V_{tp}| = 2.3\ V$

V_{out} range: $V_{cm\ min} = 0.5V$ (M_{2a})

$V_{DD} - V_{ov10} - V_{ov8} = 2.7\ V$

We let each Vov be half of their sum, and write down Id equation:

$$Id = \left(\frac{1}{2}\right)\mu n\ Cox\ \left(\frac{W}{L}\right)(Vov^2);$$

We have Id(From figure), and Vov(above),and kn'(Note.), so we can solve for W/L.

The result is below:

$k_p' = 50\ \mu A/V^2$ $k_n' = 200\ \mu A/V^2$

$|V_{tp}| = 0.7\ V$ $V_{tn} = 0.5\ V$

Set $I_b = 30\mu A$:

ICMR: $V_{ov3} + V_{tn} - |V_{tp}| = 0.5\ V$

$V_{DD} - V_{ov0} - V_{ov1a} - |V_{tp}| = 2.3\ V$

V_{out} range: $V_{cm\ min} = 0.5V$ (M_{2a})

$V_{DD} - V_{ov10} - V_{ov8} = 2.7\ V$

M_0: $2I_b = 60 = \frac{1}{2} k_p' \left(\frac{W}{L}\right) V_{ov0}^2$ (0.15V) $\Rightarrow$ $\frac{W}{L} = 106.65$

M_{1a}

M_{1b} : $\frac{I_b}{2} = 15 = \frac{1}{2} k_p' \left(\frac{W}{L}\right) V_{ov1a}^2$ (0.15V) $\Rightarrow$ $\frac{W}{L} = 26.67$

M_{2a}

M_{2b}

M_{11} : $\frac{I_b}{2} = 15 = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov11}^2$ (0.15) $\Rightarrow$ $\frac{W}{L} = 6.7$

M_{12}

M_5

M_6 : $\left(\frac{k-1}{2}\right) I_b = 30 = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov6}^2$ (0.15) $\Rightarrow$ $\frac{W}{L} = 7.5$

M_7

M_8

M_9 : $\frac{(k-1)}{2} I_b = 30 = \frac{1}{2} k_p' \left(\frac{W}{L}\right) V_{ov10}^2$ 0.15 $\Rightarrow$ $\frac{W}{L} = 53.35$

M_{10} $= I_b$

M_{3b} $\frac{I_b}{2} = 15 = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov3b}^2$ 0.3 $\Rightarrow$ $\frac{W}{L} = 1.67$

M_{4b}

M_{3a} $\frac{3I_b}{2} = 45 = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov3a}^2$ 0.3 $\Rightarrow$ $\frac{W}{L} = 5$

M_{4a}

Note: For kn' and kp', we use a single MOS as the configuration below:

And use .op with different VG to find out kp'/kn'. We use three kind of bias VG to compare our values, and pick the most reasonable value. We also use .dc and see the Id-Vg point(Vtn/Vtp can be find from the Spice Error Log) to double check.

Kn' = 200 μA/V^2

Kp' = 50 μA/V^2

The First version W/L ratio and size from our hand calculations:

Hand Calculation(Ideal)	Id(μA)	W(μm)	L(μm)	m	W/L
M0	60	14.22	4	30	106.65
M1a	15	17.78	4	6	26.67
M1b	15	17.78	4	6	26.67
M2a	15	17.78	4	6	26.67
M2b	15	17.78	4	6	26.67
M3a	45	20	4	1	5
M3b	15	6.68	4	1	1.67
M4a	45	20	4	1	5
M4b	15	6.68	4	1	1.67
M5	30	15	4	2	7.5
M6	30	15	4	2	7.5
M7	30	10.67	4	20	53.35
M8	30	10.67	4	20	53.35
M9	30	10.67	4	20	53.35
M10	30	10.67	4	20	53.35
M11	15	13.4	4	2	6.7
M12	15	13.4	4	2	6.7

Ib = 30 μA

(Note that this is ideal, we ignore body effect and channel length modulation. Spice simulation results would be more comprehensive.)

We set three bias voltage in the standard of Ib. We start from M0, for example, since we want Ib approximately = 30 microA, we first predict the Vov would be 0.15V for M0, and since VSG0= |Vov|+ |Vtn| = Vdd-Vbp1, Vbp1 約等於 2.15V. Based on hand calculation, we type down our schematics and run it on LTSpice, unfortunately, the result is not as expected. Ib is too large, and thus the Pdiss is greater than 400 microWatts. Worse yet, some transistors are not in saturation. As a result, we first fine tune the bias current to the value we want.

We want the bias current to be near 30 microA(less than and equal to), and every time we need to check whether all transistors are operated in saturation. Finally, we tune the current of M0(2Ib) to approximately **58.4 μA.**

Summarize the method we fine tune for problem 1 : We first decide the W/L from hand calculation, and pick the bias voltage we calculate, and observe the current. If the power is too high, Ib should be smaller , and thus the bias voltage Vbp1 should be greater, and vice versa.

(b)Spice Simulations

Our final sub circuit schematics : (We change K to 4 , explain later)

```
***Spice simulation Final project
.lib 'free035.l'
.global pi ni o vdd
*----Define subckt----
.subckt opamp pi ni o vdd gnd
*----I kept the syntax just in case----
*#M0 Vdd vbp1 x1 vdd mos0 w=20um l=4um m=1
*#.model mos0 NMOS (VTo=0.8 Kp=250u lambda=0.1)
***--------------------------------------
** D G S B
M0 x1 vbp1 vdd vdd pm w=19.760um l=4um m=15

M1a x2 pi x1 vdd pm w=2um l=1um m=15
M1b x3 pi x1 vdd pm w=2um l=1um m=15
M2a x5 ni x1 vdd pm w=2um l=1um m=15
M2b x4 ni x1 vdd pm w=2um l=1um m=15

M3a x2 x4 0 0 nm w=1.25um l=1um m=4
M3b x6 x4 0 0 nm w=1.25um l=1um m=1
M4a x5 x3 0 0 nm w=1.25um l=1um m=4
M4b x7 x3 0 0 nm w=1.25um l=1um m=1

M5 x8 vbn2 x2 0 nm w=3.75um l=1um m=2
M6 o vbn2 x5 0 nm w=3.75um l=1um m=2
M11 x4 vbn2 x6 0 nm w=15um l=4um m=2
M12 x3 vbn2 x7 0 nm w=15um l=4um m=2

M7 x8 vbp2 x9 vdd pm w=20um l=4um m=8
M8 o vbp2 x10 vdd pm w=20um l=4um m=8
M9 x9 x8 vdd vdd pm w=20um l=4um m=8
M10 x10 x8 vdd vdd pm w=20um l=4um m=8

Vbp1 vbp1 0 dc 2.137
Vbp2 vbp2 0 dc 1.42
Vbn2 vbn2 0 dc 1.3
.ends opamp
**----------------------**

X1 pi ni o vdd 0 opamp
cl o 0 10p
```

Spice Error Log: All Saturatoin

--- BSIM3 MOSFETS ---

Name:	m:1:12	m:1:11	m:1:6	m:1:5	m:1:4b
Model:	nm	nm	nm	nm	nm
Id:	1.42e-05	1.42e-05	4.07e-05	4.07e-05	1.42e-05
Vgs:	7.94e-01	7.94e-01	9.17e-01	9.17e-01	9.71e-01
Vds:	4.65e-01	4.65e-01	1.73e+00	1.73e+00	5.06e-01
Vbs:	-5.06e-01	-5.06e-01	-3.83e-01	-3.83e-01	0.00e+00
Vth:	6.46e-01	6.46e-01	6.41e-01	6.41e-01	5.21e-01
Vdsat:	1.32e-01	1.32e-01	2.19e-01	2.19e-01	3.17e-01
Gm:	1.61e-04	1.61e-04	2.64e-04	2.64e-04	5.66e-05
Gds:	3.96e-07	3.96e-07	6.18e-07	6.18e-07	1.45e-06
Gmb	3.92e-05	3.92e-05	6.64e-05	6.64e-05	1.54e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	7.43e-15	7.43e-15	1.79e-15	1.79e-15	2.75e-16
Cgdov:	7.38e-15	7.38e-15	1.24e-15	1.24e-15	2.74e-16
Cgbov:	8.67e-16	8.67e-16	2.07e-16	2.07e-16	1.03e-16
dQgdVgb:	4.31e-13	4.31e-13	2.70e-14	2.70e-14	4.40e-15
dQgdVdb:	-7.80e-15	-7.80e-15	-1.24e-15	-1.24e-15	-3.09e-16
dQgdVsb:	-4.09e-13	-4.09e-13	-2.47e-14	-2.47e-14	-3.88e-15
dQddVgb:	-9.27e-15	-9.27e-15	-1.25e-15	-1.25e-15	-3.49e-16
dQddVdb:	8.33e-15	8.33e-15	1.25e-15	1.25e-15	3.56e-16
dQddVsb:	1.40e-15	1.40e-15	5.96e-18	5.96e-18	1.15e-17
dQbdVgb:	-6.32e-14	-6.32e-14	-3.51e-15	-3.51e-15	-6.60e-16
dQbdVdb:	-2.18e-16	-2.18e-16	-2.49e-19	-2.49e-19	-1.92e-17
dQbdVsb:	-3.89e-14	-3.89e-14	-2.78e-15	-2.78e-15	-4.86e-16

Name:	m:1:4a	m:1:3b	m:1:3a	m:1:10	m:1:9
Model:	nm	nm	nm	pm	pm
Id:	5.57e-05	1.42e-05	5.57e-05	-4.07e-05	-4.07e-05
Vgs:	9.71e-01	9.71e-01	9.71e-01	-8.90e-01	-8.90e-01
Vds:	3.83e-01	5.06e-01	3.83e-01	-5.62e-01	-5.62e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	5.21e-01	5.21e-01	5.21e-01	-7.06e-01	-7.06e-01
Vdsat:	3.17e-01	3.17e-01	3.17e-01	-2.00e-01	-2.00e-01
Gm:	2.16e-04	5.66e-05	2.16e-04	3.81e-04	3.81e-04

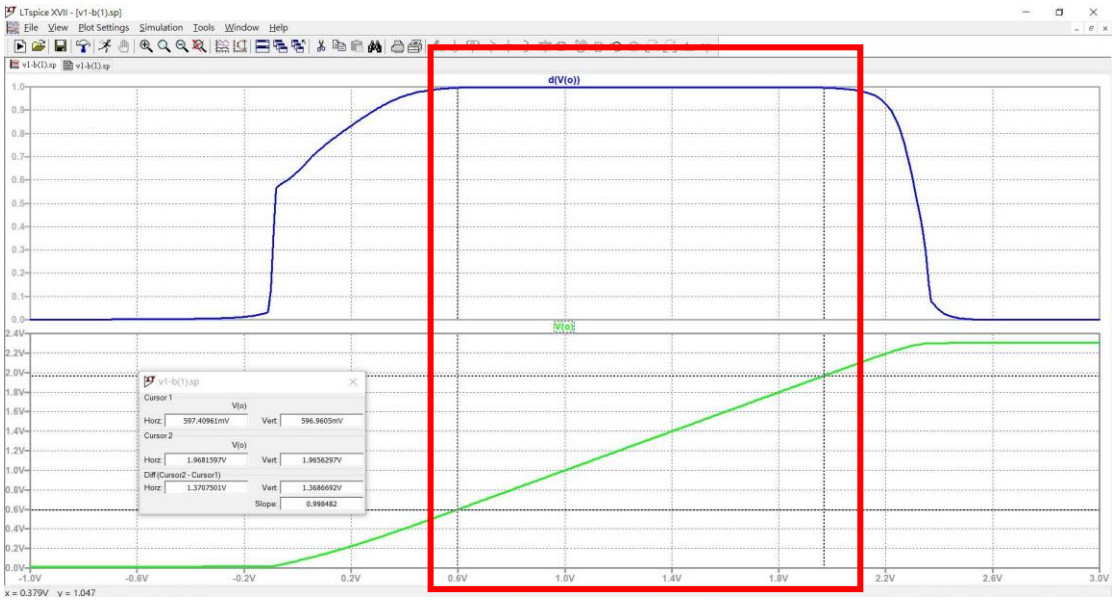
Gds:	1.62e-05	1.45e-06	1.62e-05	8.49e-07	8.49e-07
Gmb	5.92e-05	1.54e-05	5.92e-05	1.01e-04	1.01e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.10e-15	2.75e-16	1.10e-15	3.09e-14	3.09e-14
Cgdov:	1.10e-15	2.74e-16	1.10e-15	3.07e-14	3.07e-14
Cgbov:	4.14e-16	1.03e-16	4.14e-16	3.48e-15	3.48e-15
dQgdVgb:	1.79e-14	4.40e-15	1.79e-14	2.09e-12	2.09e-12
dQgdVdb:	-1.66e-15	-3.09e-16	-1.66e-15	-3.33e-14	-3.33e-14
dQgdVsb:	-1.55e-14	-3.88e-15	-1.55e-14	-1.72e-12	-1.72e-12
dQddVgb:	-2.12e-15	-3.49e-16	-2.12e-15	-4.01e-14	-4.01e-14
dQddVdb:	2.40e-15	3.56e-16	2.40e-15	3.53e-14	3.53e-14
dQddVsb:	-4.02e-17	1.15e-17	-4.02e-17	7.27e-15	7.27e-15
dQbdVgb:	-2.47e-15	-6.60e-16	-2.47e-15	-1.59e-13	-1.59e-13
dQbdVdb:	-3.07e-16	-1.92e-17	-3.07e-16	-4.76e-16	-4.76e-16
dQbdVsb:	-1.93e-15	-4.86e-16	-1.93e-15	-6.89e-13	-6.89e-13

Name:	m:1:8	m:1:7	m:1:2b	m:1:2a	m:1:1b
Model:	pm	pm	pm	pm	pm
Id:	-4.07e-05	-4.07e-05	-1.42e-05	-1.50e-05	-1.42e-05
Vgs:	-1.02e+00	-1.02e+00	-1.19e+00	-1.19e+00	-1.19e+00
Vds:	-3.28e-01	-3.28e-01	-2.19e-01	-8.07e-01	-2.19e-01
Vbs:	5.62e-01	5.62e-01	1.81e+00	1.81e+00	1.81e+00
Vth:	-8.35e-01	-8.35e-01	-1.07e+00	-1.07e+00	-1.07e+00
Vdsat:	-2.09e-01	-2.09e-01	-1.68e-01	-1.69e-01	-1.68e-01
Gm:	3.79e-04	3.79e-04	1.69e-04	1.82e-04	1.69e-04
Gds:	3.26e-06	3.26e-06	5.26e-06	8.61e-07	5.26e-06
Gmb	7.35e-05	7.35e-05	2.06e-05	2.21e-05	2.06e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.09e-14	3.09e-14	5.63e-15	5.63e-15	5.63e-15
Cgdov:	3.09e-14	3.09e-14	5.62e-15	5.59e-15	5.62e-15
Cgbov:	3.48e-15	3.48e-15	1.57e-15	1.57e-15	1.57e-15
dQgdVgb:	2.08e-12	2.08e-12	9.91e-14	9.61e-14	9.91e-14
dQgdVdb:	-5.45e-14	-5.45e-14	-7.68e-15	-5.56e-15	-7.68e-15
dQgdVsb:	-1.73e-12	-1.73e-12	-7.85e-14	-7.72e-14	-7.85e-14
dQddVgb:	-8.76e-14	-8.76e-14	-1.05e-14	-5.72e-15	-1.05e-14
dQddVdb:	7.08e-14	7.08e-14	8.96e-15	5.63e-15	8.96e-15

dQddVsb:	2.75e-14	2.75e-14	2.10e-15	1.04e-16	2.10e-15
dQbdVgb:	-1.12e-13	-1.12e-13	-3.98e-15	-4.15e-15	-3.98e-15
dQbdVdb:	-3.03e-15	-3.03e-15	-1.06e-16	1.30e-17	-1.06e-16
dQbdVsb:	-5.52e-13	-5.52e-13	-1.90e-14	-1.90e-14	-1.90e-14

Name:	m:1:1a	m:1:0
Model:	pm	pm
Id:	-1.50e-05	-5.84e-05
Vgs:	-1.19e+00	-8.63e-01
Vds:	-8.07e-01	-1.81e+00
Vbs:	1.81e+00	0.00e+00
Vth:	-1.07e+00	-7.06e-01
Vdsat:	-1.69e-01	-1.78e-01
Gm:	1.82e-04	6.18e-04
Gds:	8.61e-07	5.19e-07
Gmb	2.21e-05	1.65e-04
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	5.63e-15	5.73e-14
Cgdov:	5.59e-15	3.76e-14
Cgbov:	1.57e-15	6.52e-15
dQgdVgb:	9.61e-14	3.83e-12
dQgdVdb:	-5.56e-15	-3.77e-14
dQgdVsb:	-7.72e-14	-3.16e-12
dQddVgb:	-5.72e-15	-3.84e-14
dQddVdb:	5.63e-15	3.78e-14
dQddVsb:	1.04e-16	9.05e-16
dQbdVgb:	-4.15e-15	-3.01e-13
dQbdVdb:	1.30e-17	-1.33e-17
dQbdVsb:	-1.90e-14	-1.27e-12

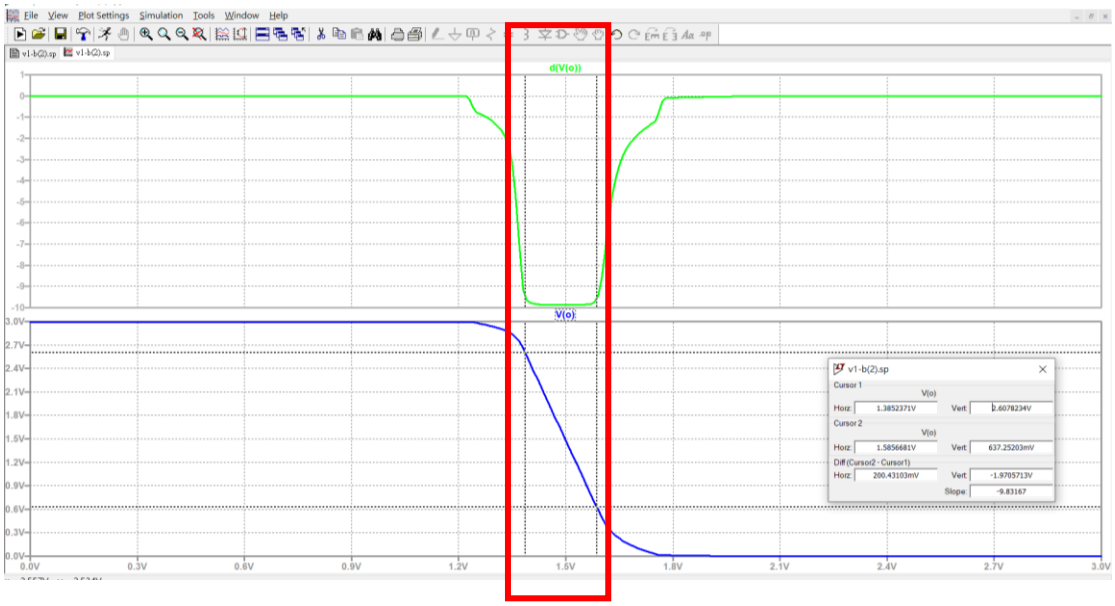
(1) ICMR



ICMR : 0.5V <= Vcm <=1.96V

We didn't have much difficulties in meeting the spec of Input Common Mode Range, but there's one thing worth discussion. In order to confirm the real linear region, we differentiate the Vout and get the horizontal (constant) region. Note that our the Vcm,max could not reach 2.3V.

(2) Output range



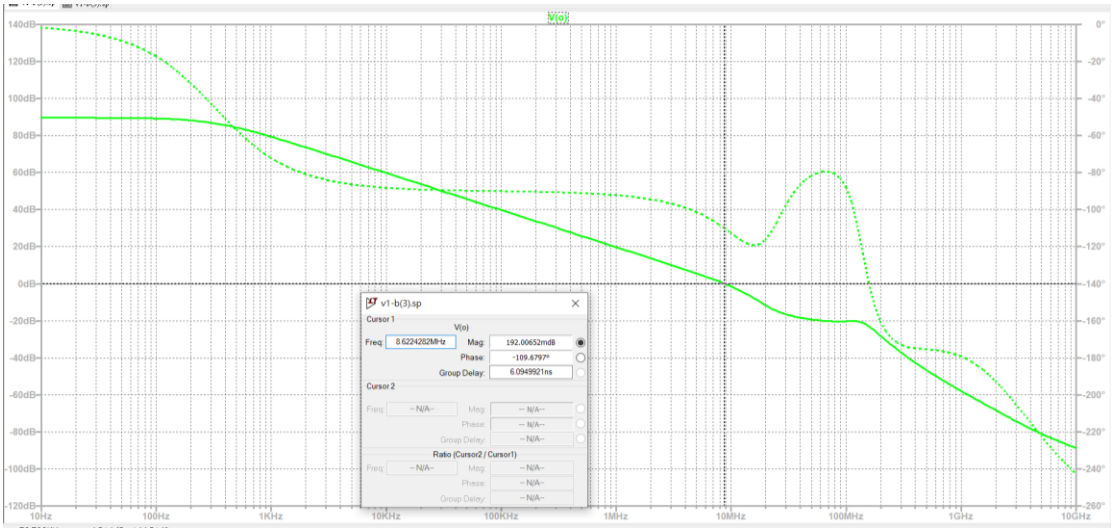
Output range : 0.6V <= Vout <= 2.6V

Same as ICMR, we differentiate Vout and choose the constant dVout region. The output range can almost meet the spec.

Our Vout can swing from about 0.6V to 2.6V.

(3) Open-loop frequency response, AV, GB, and PM

The K=3 version :



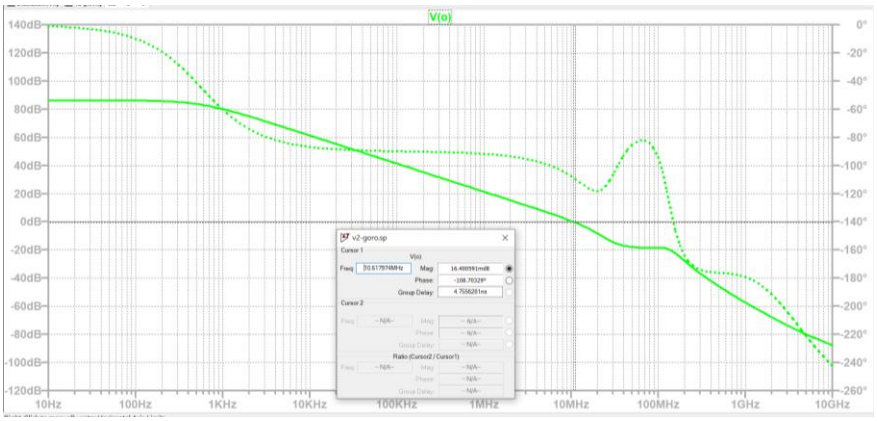
Av = 89.482227dB

GB =8.7671496MHz @ 270.04169µdB

PM = 180 -110.00065° = 70°

We observe that the Gain is ok, and so is the phase margin, but the bandwidth is to small. We try to think how to extend bandwidth. If we can move the dominant pole more to the right, which means the RC time constant should be smaller, the one over RC would be farther. First pole would be decide by CL and output resistance, which is very large. The second pole is determined by M3a : M3b / M4a : M4b current mirrors. We want to extend bandwidth, so we try to make this pole farther. The resistance of this RC is the resistance looking into the folded node.(x2 or x5 in our schematics.) In order to make Rc smaller, the $Rox2 = ro1a \,||\, ro3a \,||\, ((ro5 + RL5)/Avo5)$, ro = VA / Id. If we want Rox2 become smaller, we can let ro3a smaller, so we modify K to 4. Once the Rox2 became smaller, the GB became larger.

The K=4 version :



Av = 86.136484dB

GB = 10.61MHz

PM = 71.2°

GB @16.4mdB(the closest to 0dB) : 10.61MHz, PM still 71.2° >70°

Why don't we increase the m or the ratio as large as possible? If the W/L is to large, the Vov of M3a~M4b would be very small (0.08V), once Vov are too small, the linearity is not very good. The phase margin would somehow decreased if we increase the W/L to very large. For experiment, I set their m to be: 8000 / 2000 (K still = 4), and see the result:

The Phase is -160 degree and PM only 20! Worse yet, the GB decay to 5.49 MHz. The reason might be that when the W/L ratio is too large, the capacitance would be very large, so time constant increase, and thus pole and GB become smaller.

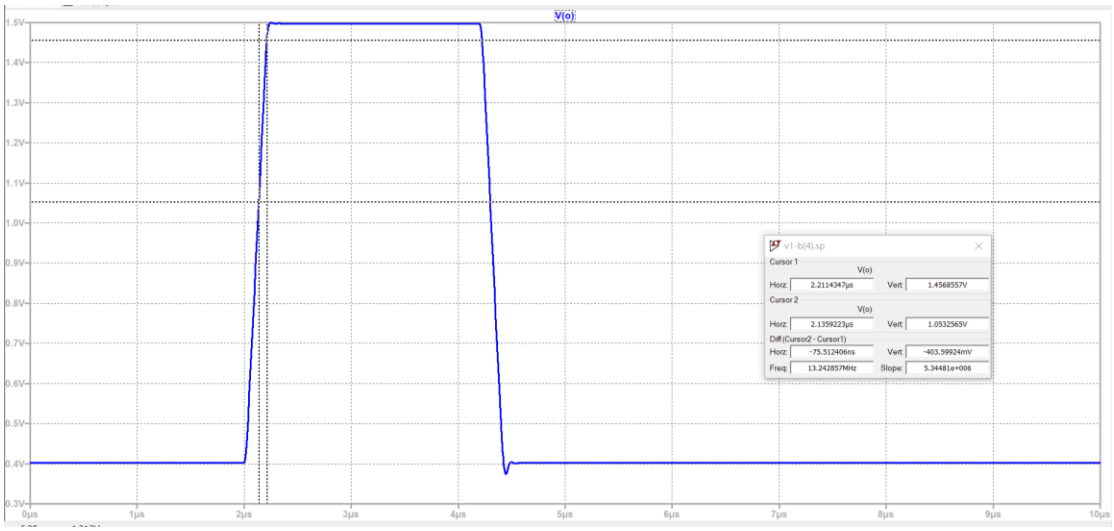
Also, if we increase W/L, then Vov would be very small, and gm (2Id/Vov) would increase. If gm becomes infinitely large, then output resistance :

$$Rout = gm6ro6(ro2||ro4)||gm8ro8ro10$$

would be very large, the wp1 (first pole = 1/RoutCL) would be smaller, so the GB would decrease.

(4) positive and negative slew rates

Initially, our .tran simulation get really bad result. The magnitude can not reach 1.5V, and only have several mV magnitude. This is really strange. We check everything : Saturation, Symmetry, try to raise W/L… all don't work. Later we find out that the time we set is too small to let the circuit respond. The correct code $.trans\ 0\ 10us$ where we type *10ns*, after we fixed this problem, the problem solved.



-					
us	4.349776 V 4.282511	0.770797 RATIO 1.145458	-0.37466 slew rate 0.067265		-5.56995
+					
us	2.139738 V 2.101528	1.074188 RATIO 0.864627	0.209561 slew rate 0.03821		5.48451

From the figure above, (unit : V/μs) our SR is greater than the spec, meaning that our circuit responds to the input relatively fast, and wouldn't delay very significant.

(5) PSRR+ and PSRR- of the Op-amp

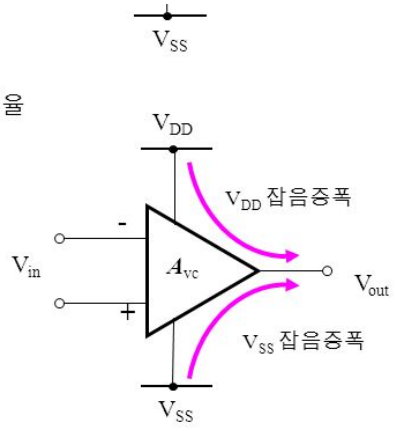
PSRR is the power supply rejection ratio, according to the formula :

(3-10) Power supply rejection ratio (*PSRR*)

- 전원단자에 나타나는 noise 신호등의 증폭 이득 제거율

$$PSRR+ = \frac{A_{vd}}{V_o / V_{DD}}$$

$$PSRR- = \frac{A_{vd}}{V_o / V_{SS}}$$



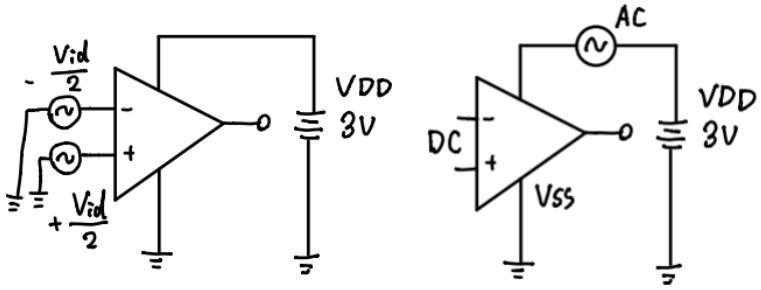
We design two circuits below, and run the simulation.

We instantiate two sub circuits, and give them independent source, and then type expression :

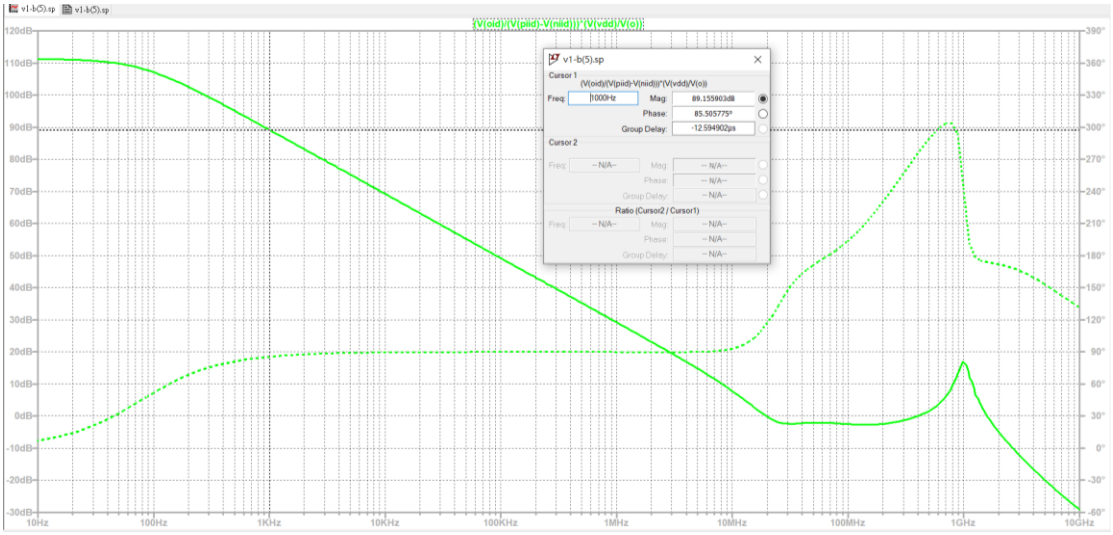
$$\frac{V_{oid})}{(V_{piid}-V_{niid})} \times \frac{V_{vdd}}{V_o}$$

Circuit design

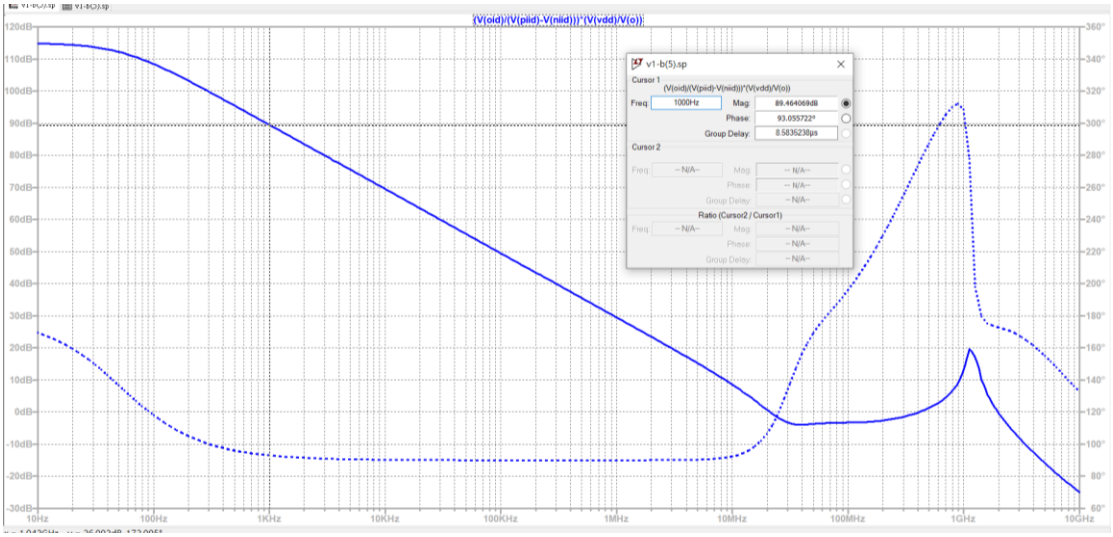
PSRR+:



Our PSRR+ increase as we increase K from 3 to 4.



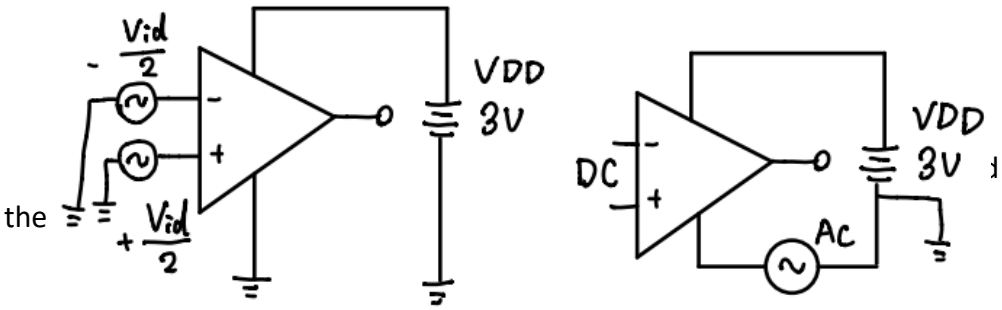
PSRR+ : 89.15dB



PSRR+ 89.46dB

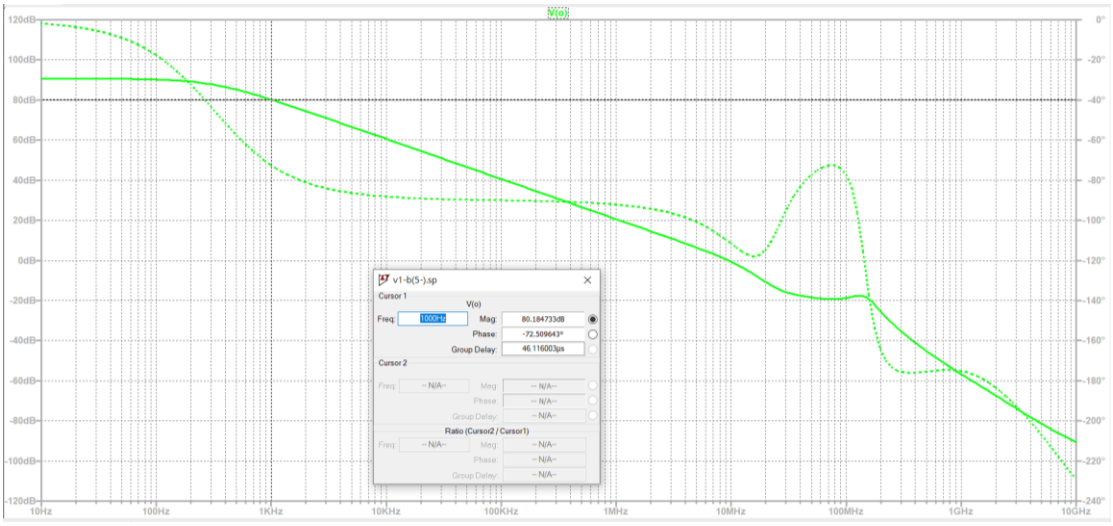
Circuit design

PSRR-:

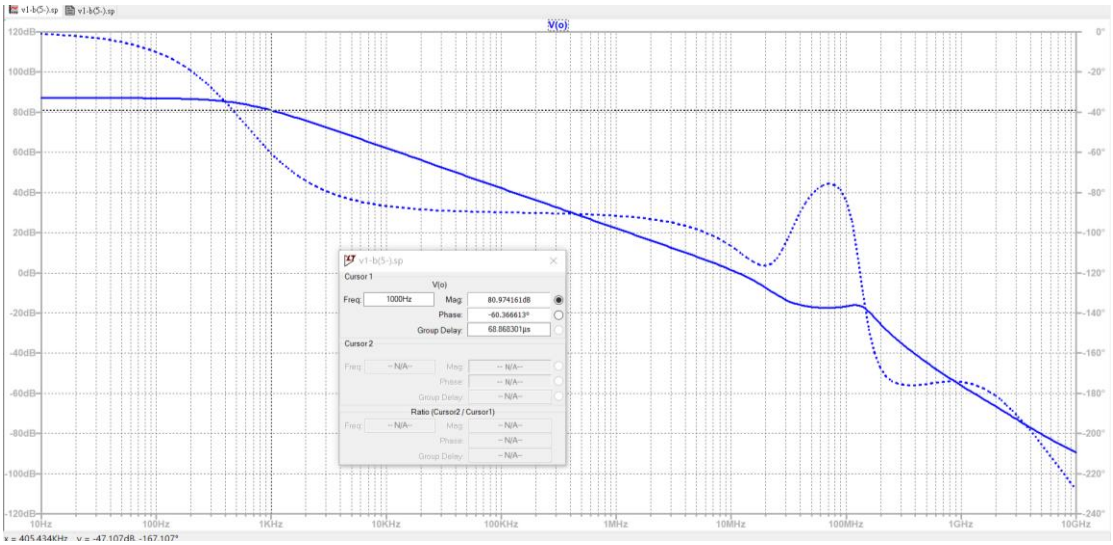


the

$$\frac{V(oid)}{(V_{piid}-V_{niid})} \times \frac{V_{vss}}{V_o}$$



PSRR- : 80.2dB



PSRR- : 80.97dB

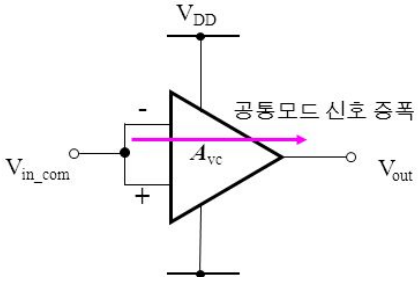
Our PSRR- increase as we increase K from 3 to 4.

(6) CMRR

(3-9) Common mode rejection ratio (*CMRR*)

• 공통 모드 입력 신호의 증폭 이득 제거율

$$CMRR = \frac{A_{vd}}{A_{vc}}$$



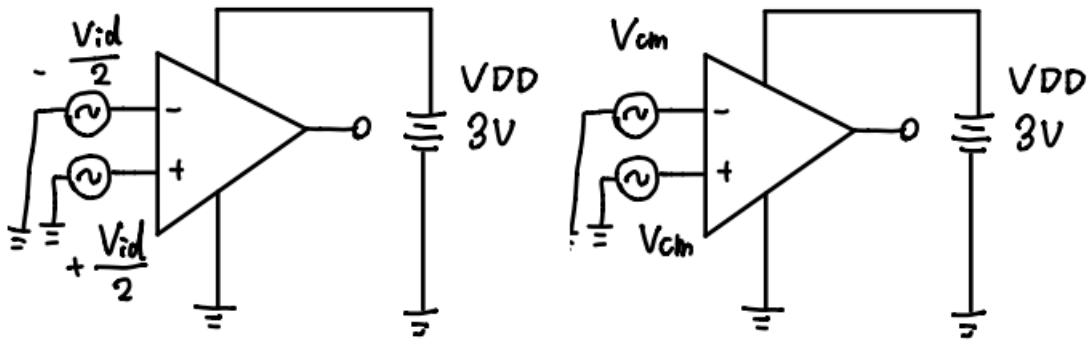
The spec required CMRR >= 40dB before meeting unity-gain frequency,

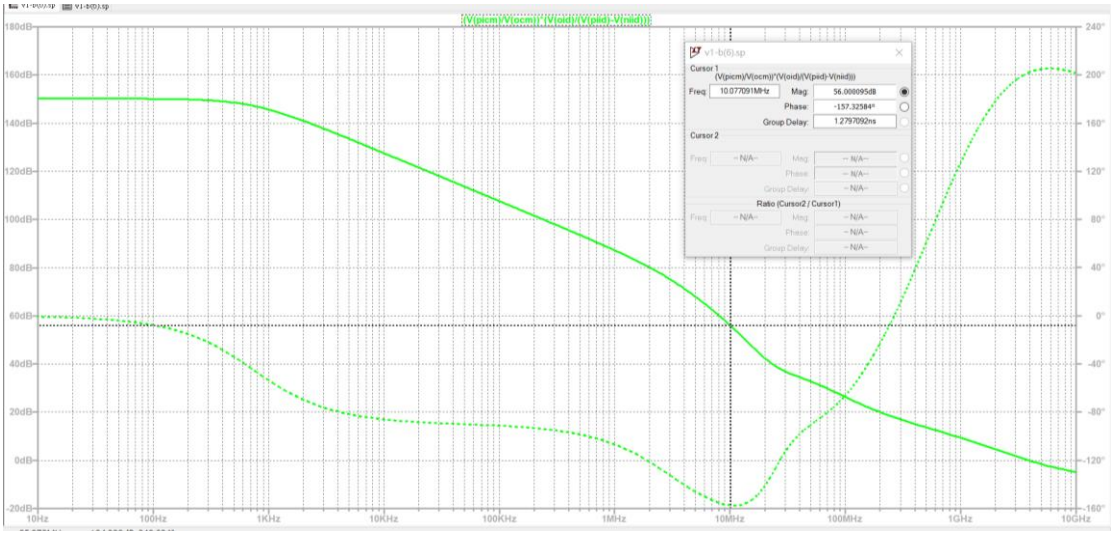
luckly, our CMRR remained >=40dB all the way down to ft, so there's no too much tuning here. We hope the common mode rejection performance would be as well as simulation results.

We instantiate two sub circuits, and give them independent source, and then type expression :

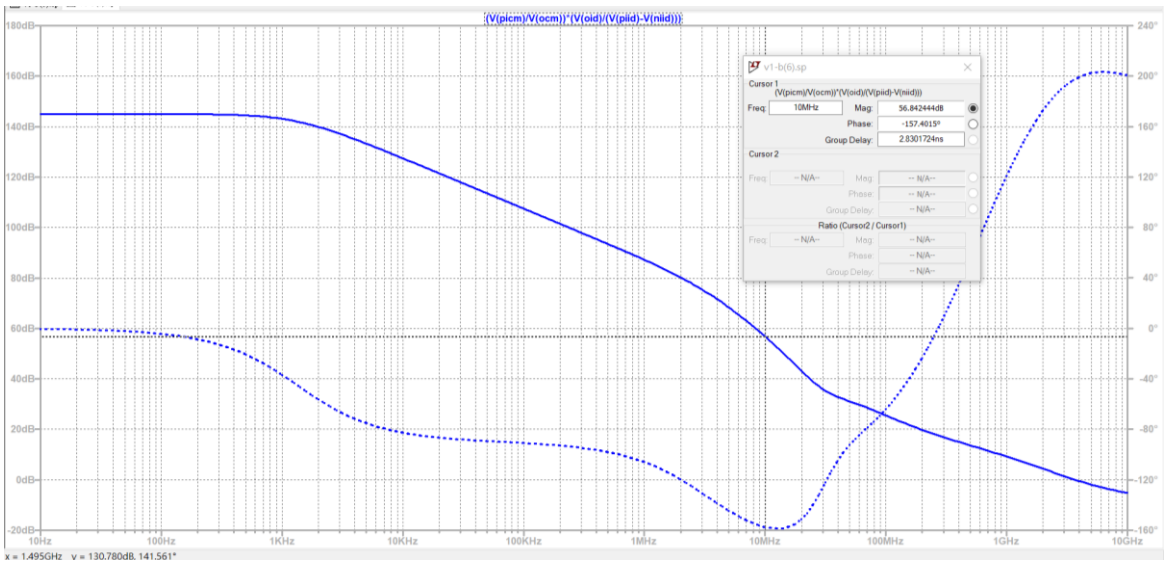
$$\frac{V_{picm}}{V_{ocm}} \times \frac{V_{oid}}{(V_{piid}-V_{niid})}$$

Circuit design





CMRR@10MHz : 56.12dB



CMRR@10MHz 56.84dB

(7) Final Table of size

Final Design	W(μm)	L(μm)	m	W/L
M0	19.76	4	15	74.1
M1a	2	1	15	30
M1b	2	1	15	30
M2a	2	1	15	30
M2b	2	1	15	30
M3a	1.25	1	4	5
M3b	1.25	1	1	1.25
M4a	1.25	1	4	5
M4b	1.25	1	1	1.25
M5	3.75	1	2	7.5
M6	3.75	1	2	7.5
M7	20	4	8	40
M8	20	4	8	40
M9	20	4	8	40
M10	20	4	8	40
M11	15	4	2	7.5
M12	15	4	2	7.5

(c) Summarize spec met by our designs.

Specifications	Value	Units
Pdiss	438	μW
ICMR	0.5 <= ICMR <=1.96	V
Vout	0.6 <= Vout <= 2.6	V
Av	86.13	dB
GB	10.61	MHz
PM	71.2	°
PSRR+(@1KHz)	89.46	dB
PSRR-(@1KHz)	80.97dB	dB
CMRR	56.84	dB
Slew rate +	5.48	V/μs
Slew rate -	-5.57	V/μs
Vbp1	2.137	V
Vbp2	1.42	V
Vbn2	1.3	V

Ib : 29.2 μA

To sum up, we increase K from 3 to 4, though the power consumption is a little bit higher than the spec, but other performances improve. We sacrifice the power (a little!!!) to obtain better overall performance.

2. Simulation Code :

```
Simulation code

**ICMR
X1 pi ni o vdd 0 opamp
cl o 0 10p
rl o 0 1000k
VDD vdd 0 dc 3
VSS vss 0 dc 0
Vip pi 0 dc 3
Vin ni o dc 0
.op
.dc Vip -1 3 0.01
.end

**OUTPUT RANGE
X1 pi ni o vdd 0 opamp
cl o 0 10p
rl o 0 1000k
rl2 ni vin 10000k
rl3 ni o 100000k
VDD vdd 0 dc 3
VSS vss 0 dc 0
Vref pi 0 dc 1.5
Vin vin 0 dc 3
.op
.dc Vin 0 3 0.01
.end

**Av ,GB,PM
X1 pi ni o vdd 0 opamp
cl o 0 10p
VDD vdd 0 dc 3
Vin pi ni dc 0 ac 1
.op
.ac dec 20 10 10G
.end
```

```
**SR
X1 pi ni o vdd vss opamp
Cl o 0 10p
Rl o 0 1000k

Vni ni o dc 0
Vpi pi 0  pulse (0.4 1.5 2u 0 0 2u 4u 1)
Vdd vdd 0 dc 3
Vss vss 0 dc 0
.op
.tran 0 10us
.end
**PSRR+

X1 pi ni o vdd vss opamp
cl o 0 10p

VDD vdd 0 dc 3 ac 0.5
VSS vss 0 dc 0
Vpi pi 0 dc 1.5
Vni ni 0 dc 1.5

X2 piid niid oid vddid vssid opamp
cl2 o id 0 10p

VDDid vddid 0 dc 3
VSSid vssid 0 dc 0
Vpiid piid 0 dc 1.5 ac 0.5
Vniid niid 0 dc 1.5 ac -0.5
.op
.ac dec 20 10 10G
.end

**PSRR-
X1 pi ni o vdd vss opamp
cl o 0 10p
VDD vdd 0 dc 3
VSS vss 0 dc 0 ac 1
Vpi pi 0 dc 1.5 ac 0.5
Vni ni 0 dc 1.5 ac -0.5
.op
.ac dec 20 10 10G
```

```
**CMRR
Xcm picm nicm ocm vddcm 0 opamp
clcm ocm 0 10p
VDDcm vddcm 0 dc 3
VSScm vsscm 0 dc 0
Vpicm picm 0 dc 1.5 ac 1
Vnicm nicm 0 dc 1.5 ac 1

Xid piid niid oid vddid 0 opamp
clid oid 0 10p
VDDid vddid 0 dc 3
VSSid vssid 0 dc 0
Vpiid piid 0 dc 1.5 ac 0.5
Vniid niid 0 dc 1.5 ac -0.5
.op
.ac dec 20 10 10G
.end
```